



128Kx32 SRAM MODULE, SMD 5962-93187

FEATURES

- Access Times of 70, 85, 100, 120ns
- MIL-STD-883 Compliant Devices Available
- Packaging
 - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400).
 - 68 lead, 40mm Low Profile CQFP, 3.56mm (0.140") (Package 502).
 - 68 lead, Hermetic CQFP (G2U), 22.4mm (0.880 inch) square, 4.57mm (0.140 inch) high, (Package 510)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS128K32-XG2UX - 8 grams typical
 - WS128K32-XH1X - 13 grams typical
 - WS128K32-XG4TX - 20 grams typical
- Upgradeable to 512Kx32

FIGURE 1 – PIN CONFIGURATION FOR WS128K32N-XH1X

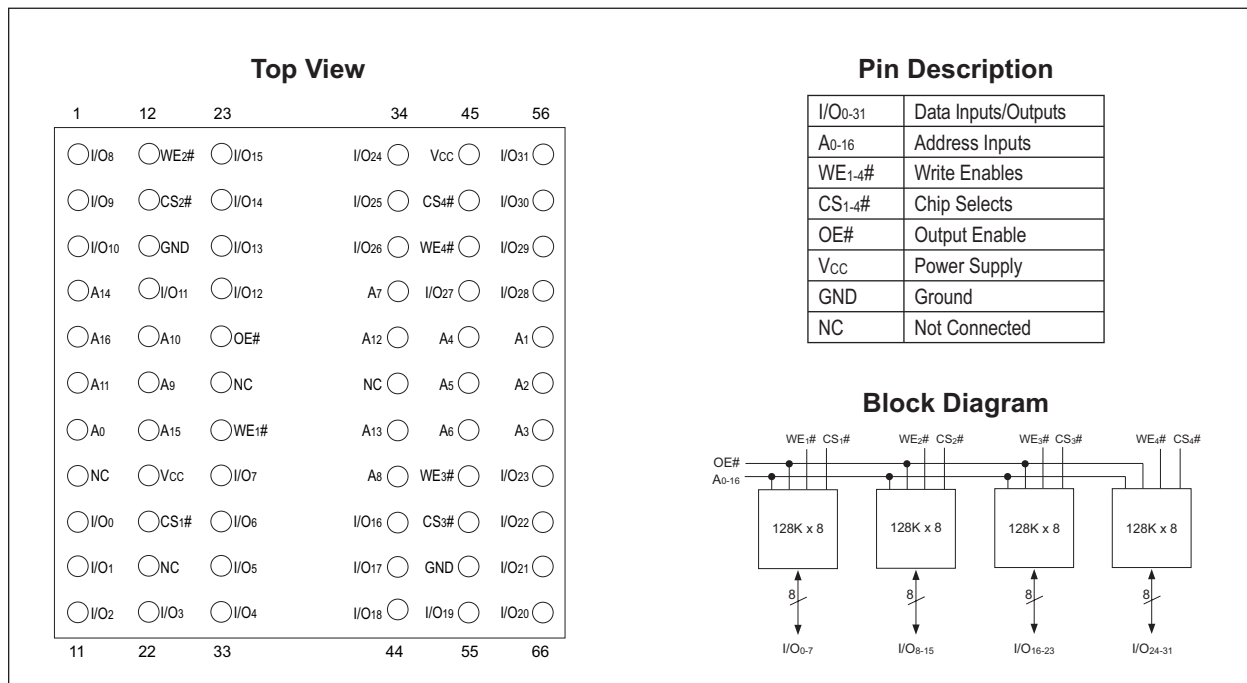




FIGURE 2 – PIN CONFIGURATION FOR WS128K32-XG4TX

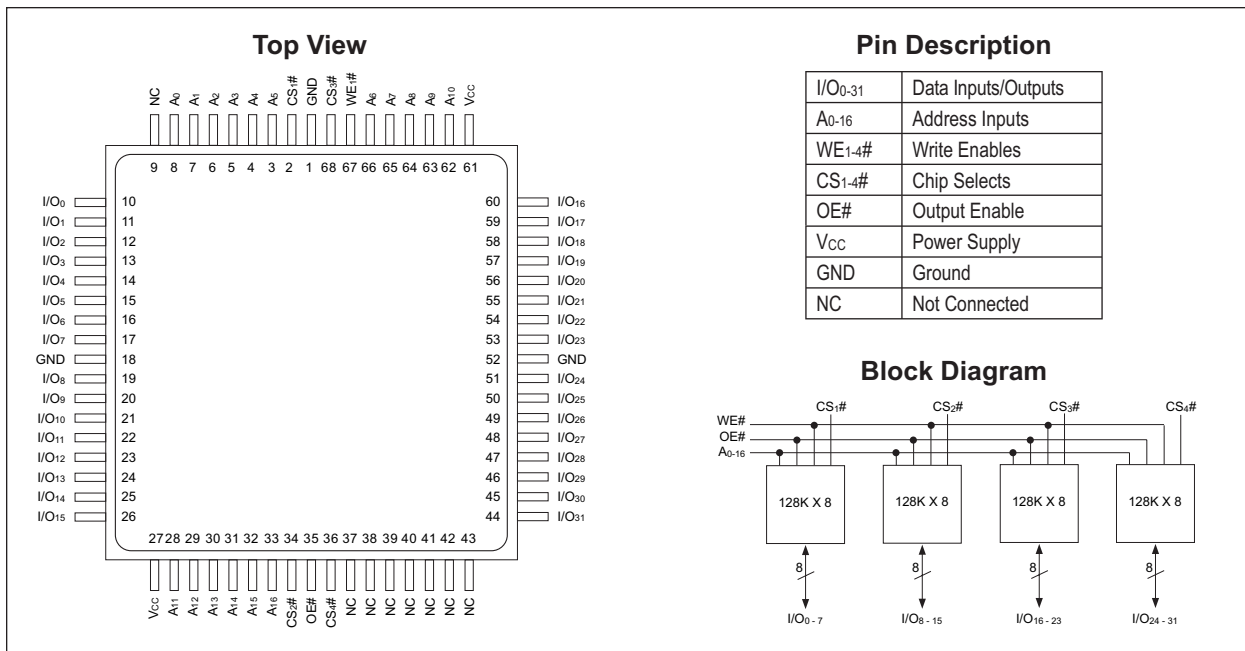
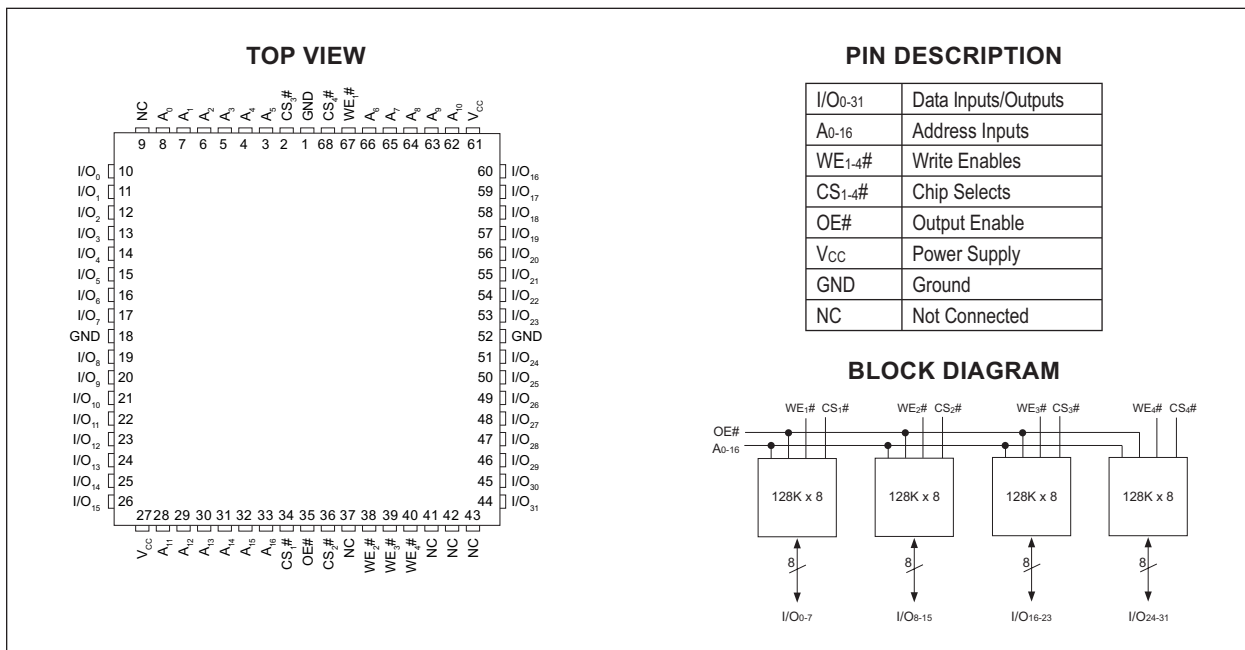
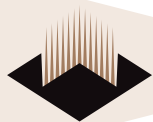


FIGURE 3 – PIN CONFIGURATION FOR WS128K32-XG2UX





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C _{OE}	V _{IN} = 0V, f = 1.0 MHz	50	pF
WE1-4# capacitance HIP (PGA)	C _{WE}	V _{IN} = 0V, f = 1.0 MHz	20	pF
CQFP G4T			50	
CQFP G2U			15	
CS1-4# capacitance	C _{CS}	V _{IN} = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	C _{I/O}	V _{I/O} = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

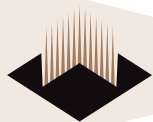
Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10		10		10		10	μA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10		10		10		10	μA
Operating Supply Current	I _{CC}	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5		120		120		120		120	mA
Standby Current	I _{SB}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5		20		20		20		20	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 4.5	2.4		2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

-55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Data Retention Supply Voltage	V _{DR}	CS ≥ V _{CC} - 0.2V	2.0	5.5	2.0	5.5	2.0	5.5	2.0	5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		4		4		4		4	mA



AC CHARACTERISTICS

$V_{CC} = 5.0V$, $GND = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Select Access Time	t_{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t_{OE}		35		45		50		60	ns
Chip Select to Output in Low Z	t_{CLZ}^1	3		3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}^1	0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}^1		25		25		35		35	ns
Output Disable to Output in High Z	t_{OHZ}^1		25		25		35		35	ns

AC CHARACTERISTICS

$V_{CC} = 5.0V$, $GND = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		75		80		100		ns
Address Valid to End of Write	t_{AW}	60		75		80		100		ns
Data Valid to End of Write	t_{DW}	30		35		40		50		ns
Write Pulse Width	t_{WP}	50		55		70		80		ns
Address Setup Time	t_{AS}	5		5		5		5		ns
Address Hold Time	t_{AH}	5		5		5		5		ns
Output Active from End of Write	t_{OW}^1	5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}^1		25		25		35		35	ns
Data Hold Time	t_{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIGURE. 4 – AC TEST CIRCUIT

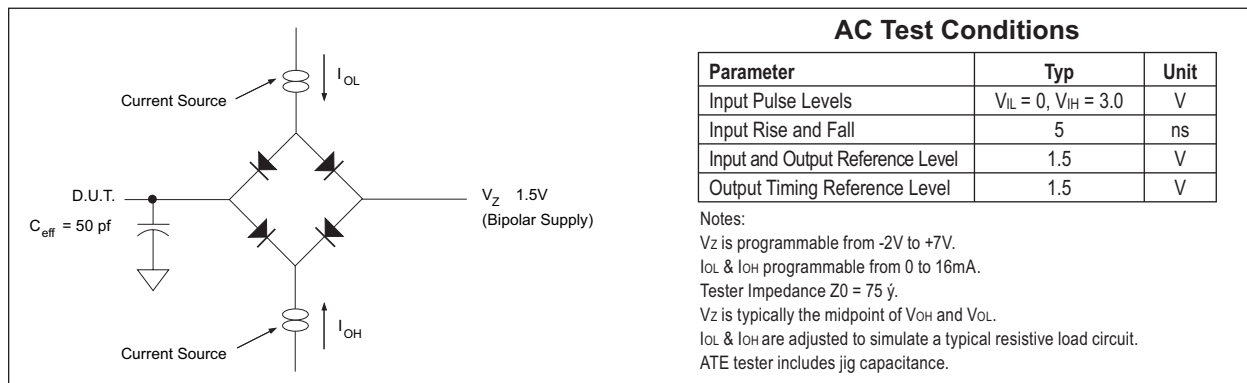




FIGURE 5 – TIMING WAVEFORM - READ CYCLE

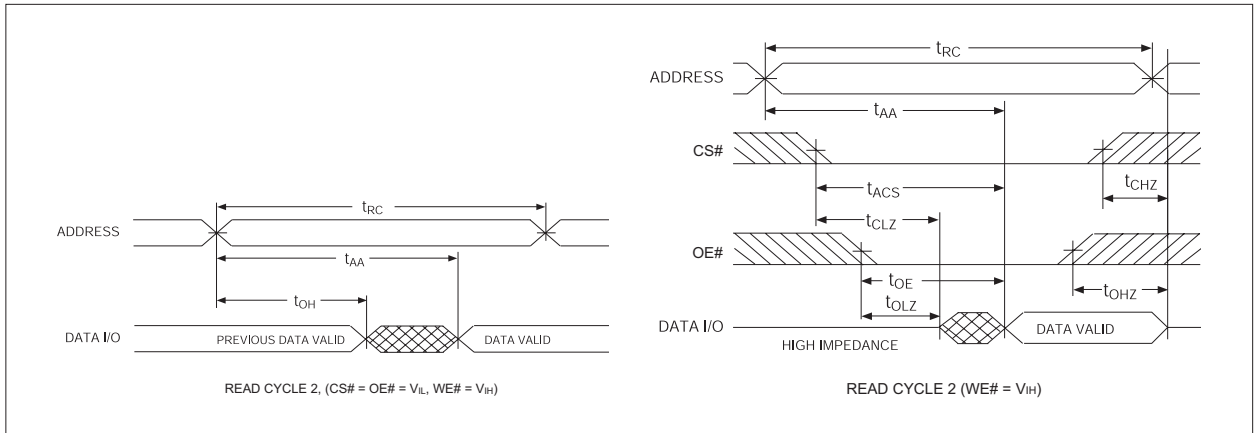


FIGURE 6 – WRITE CYCLE - WE# CONTROLLED

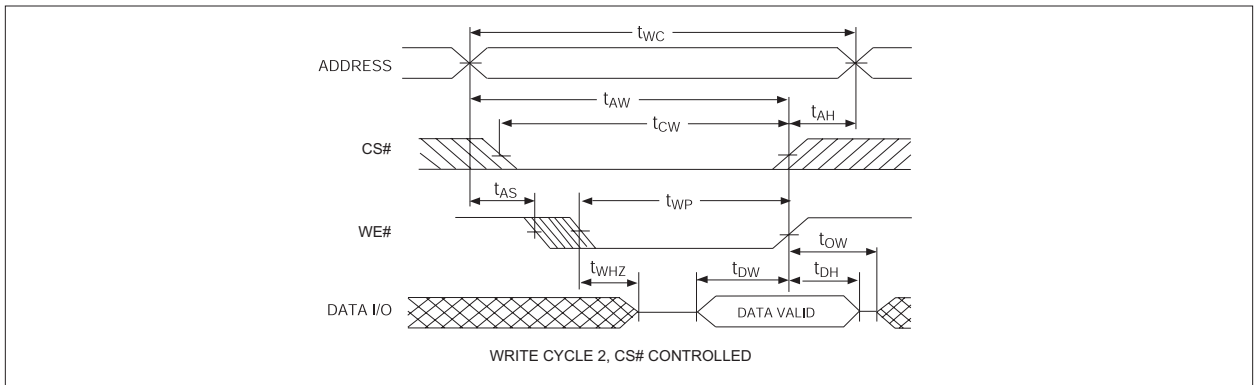
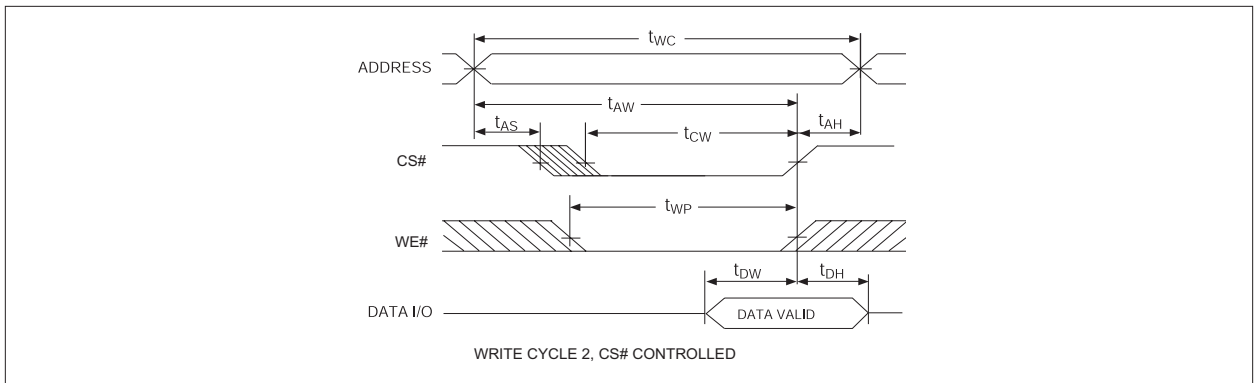
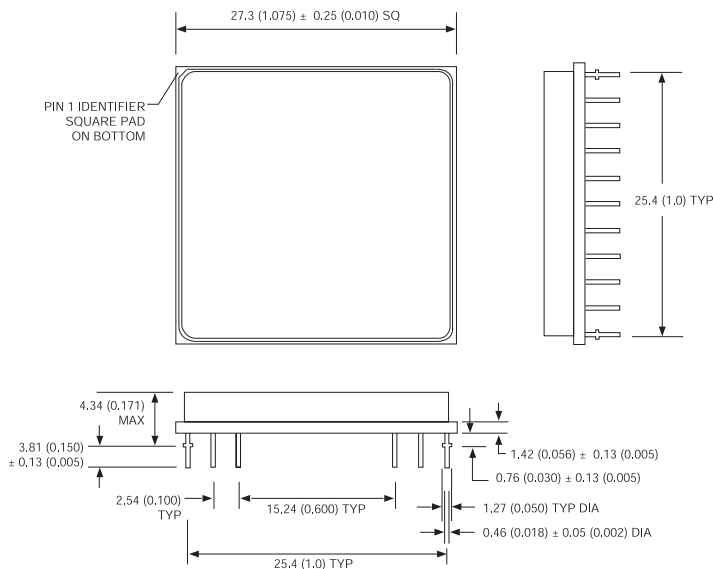
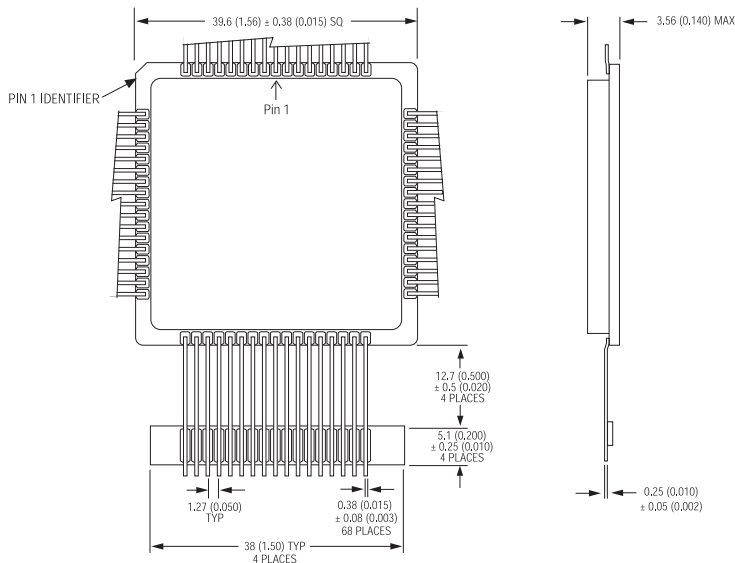


FIGURE 7 – WRITE CYCLE - CS# CONTROLLED



**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)¹

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



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ORDERING INFORMATION

W S 128K 32 X - XXX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

H1 = 1.075" sq. Ceramic Hex-In-line Package, HIP (Package 400)

G2U = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 510)

G4T = 40 mm Low Profile CQFP (Package 502)

ACCESS TIME (ns)

IMPROVEMENT MARK:

N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE ELECTRONIC DESIGNS CORPORATION



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 SRAM Module	120ns	66 pin HIP (H1)	5962-93187 01H5X
128K x 32 SRAM Module	100ns	66 pin HIP (H1)	5962-93187 02H5X
128K x 32 SRAM Module	85ns	66 pin HIP (H1)	5962-93187 03H5X
128K x 32 SRAM Module	70ns	66 pin HIP (H1)	5962-93187 04H5X
128K x 32 SRAM Module	120ns	68 lead CQFP/J (G2U)	5962-95595 01HNX
128K x 32 SRAM Module	100ns	68 lead CQFP/J (G2U)	5962-95595 02HNX
128K x 32 SRAM Module	85ns	68 lead CQFP/J (G2U)	5962-95595 03HNX
128K x 32 SRAM Module	70ns	68 lead CQFP/J (G2U)	5962-95595 04HNX
128K x 32 SRAM Module	120ns	68 lead CQFP Low Profile (G4T)	5962-95595 01HYX
128K x 32 SRAM Module	100ns	68 lead CQFP Low Profile (G4T)	5962-95595 02HYX
128K x 32 SRAM Module	85ns	68 lead CQFP Low Profile (G4T)	5962-95595 03HYX
128K x 32 SRAM Module	70ns	68 lead CQFP Low Profile (G4T)	5962-95595 04HYX